A Bandgap Reference Source for Buck DC-DC Converter

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Abstract: Aiming at the widely used Buck DC-DC converter, a negative feedback loop for Buck DC-DC power management system is designed in this paper, considering the influence of the voltage accuracy generated by the bandgap reference source on the system output. Based on the analysis of the traditional BJT-based voltage reference source, this paper selects TSMC 65nm CMOS process and performs simulation in the temperature range of -40℃ to 90℃. When the input voltage is 5V, the temperature coefficient of the reference source is $5.3\times10^{-6}\,ppm/℃$, and power supply rejection ratio(PSRR) is -65.8dB@dc, all of which show good performance.

1. Introduction

With the development of Buck DC-DC converter towards high current and high frequency, this also places essential requirements on the bandgap reference circuit. The heavy current of the converter means that the power consumption of the entire system will be increased, so the reference circuit needs to work in a relatively wide temperature range, and as far as possible to ensure that the output reference voltage keeps relatively small fluctuations; high frequency refers to that the entire converter work at higher frequencies, and the various output indicators are relatively stable. In the design of the DC-DC converter, the reference current and voltage of the under-voltage closed-loop latch, error amplifier, etc. are all generated by the bandgap reference circuit. The accuracy of this reference will directly affect the relevant output reference signal, therefore affecting the accuracy of the entire circuit[1]. The ripple or noise of the power supply is input into the bandgap reference, and the output voltage of this reference source will use as a differential input to the error amplifier. This part regarded as the ripple or noise in the input signal, will be amplified, which will affect the stable performance of the entire system. So it is necessary to consider the influence of temperature, frequency and the power supply rejection ratio characteristics[1]. In this way, the reference circuit can normally work, so that the entire converter can maintain a stable working state, thereby outputting a reliable step-down signal.

Based on the analysis of the traditional BJT voltage reference source, the circuit designed in this paper uses TSMC 65nm CMOS technology. After theoretical analysis and system simulation, the bandgap reference circuit is a reference circuit (-40℃~90℃), operated at higher frequencies (up to1.5MHz), and low PSRR (-65.8dB at low frequencies and -40.2dB at high frequencies). This circuit can also provide a stable reference voltage for the Buck DC-DC converter.

2. Principle Of Bandgap Reference Circuit

The module of the bandgap reference source establishes a voltage or current mechanism in Buck DC-DC converter, which is independent of power supply voltage and device technology, so that the bandgap will have a specific temperature characteristic[2]. The reference source circuit is based on the zero-temperature of the semiconductor material. The negative temperature characteristics provided by a single bipolar transistor and the positive temperature characteristics of the different levels ΔV_{BE} of two identical transistors, they are added with appropriate weights. Then will export zero-correlation attributes of the reference voltage:

$$V_{ref} = V_{BE} + \alpha \Delta V_{BE} = V_{BE} + \alpha V_T \ln N \tag{1}$$

Where N is the ratio of the of two transistors' number connected in parallel; α is a constant; V_T is the thermal voltage $(V_T = \kappa T / q)$, κ is the Boltzmann coefficient, q is the magnitude of unit charge; T is the absolute temperature (generally 300 Kelvin). Let $K = \alpha \ln N$, then Eq. (1) becomes

$$V_{ref} = V_{BE} + KV_T \tag{2}$$

The traditional bandgap reference is shown in Fig.1:

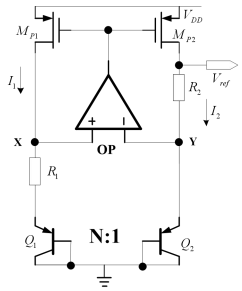

Figure 1: The traditional bandgap voltage reference.

In Fig. 1, the "virtual short" principle of the OP(operational amplifier) AMP is: $V_X = V_Y$. Then there are:

$$V_{BE,Q1} + R_1 I_1 = V_{BE,Q2} \tag{3}$$

Basic knowledge by BJT [2]: $\Delta V_{BE} = V_T \ln N$. Where N is the ratio of the number of two transistors connected in parallel. Then:

$$
\begin{aligned}
V_{R1} &= R_1 I_1 \\
&= V_{BE,Q2} - V_{BE,Q1} \\
&= \Delta V_{BE}
\end{aligned}
\tag{4}
$$

The output voltage is:

$$
\begin{aligned}
V_{ref} &= V_{BE,Q2} + \frac{V_T \ln N}{R_1} R_2 \\
&= V_{BE,Q2} + V_T \frac{R_2}{R_1} \ln N
\end{aligned}
\tag{5}
$$

Let $K = (R_2 / R_1) \ln N$, it can be found that Eq. (5) and Eq. (2) are equal. Among Eq. (5), when the value of N is determined, the positive and negative temperature coefficients can be canceled by selecting an appropriate ratio of the two resistances R_1、R_2, so that a reference voltage with zero temperature-dependent change can be obtained[2].

3. Bandgap Reference Structure

As shown in Fig. 2, it is the whole structure circuit of the bandgap reference voltage source proposed in this paper. The whole circuit mainly includes the following three parts: (a)the reference start and bias module, (b)the bandgap reference core module, (c)the negative feedback loop module.

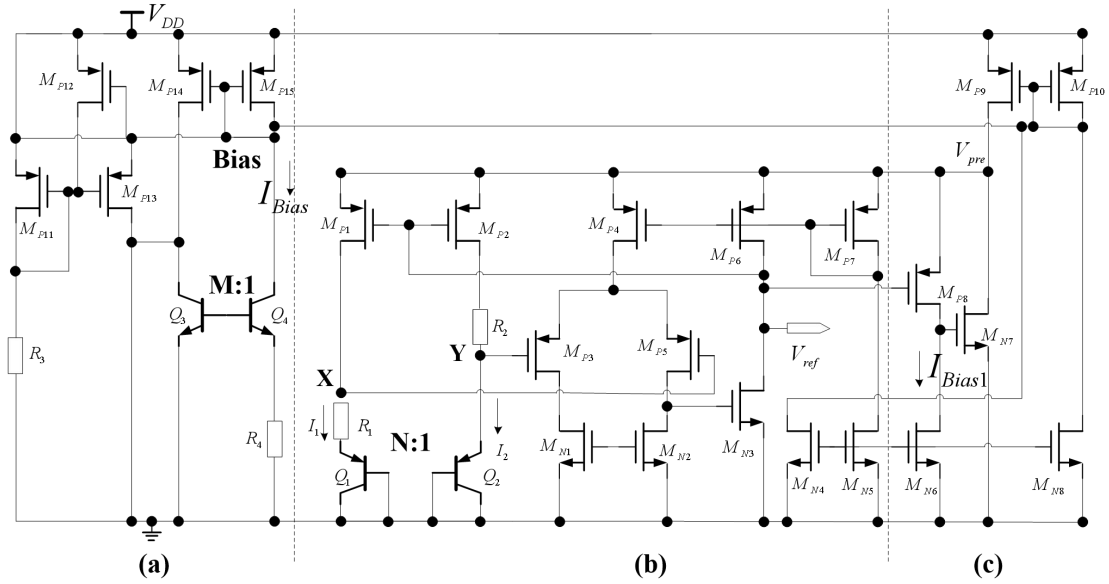

Figure 2: Bandgap reference circuit proposed in this paper.

3.1.Reference Startup and Bias Circuit

When the reference source circuit is working, there are generally two balanced operating points, namely: the zero point and the normal operating point. In order to get the entire reference source circuit out of this typically zero operating state, it is necessary to design a starting circuit for this system. Thus, the reference circuit can enter a normal working state. In Fig. 2, the MOS transistors M_{P11}、M_{P12}、M_{P13} and resistor R_3 form the starting circuit of the reference source. MOS transistor

M_{P11} is a diode connection method. When the system is powered on, M_{P11} turns on, and the power supply voltage and resistance R_3 jointly determine its' current magnitude. A current mirror is formed by MOS transistors M_{P11} and M_{P13}, thus the current of MOS transistor M_{P13} can drive the transistors Q_3、Q_4 and turns them on. A PATA (Proportional to the Absolute Temperature) current, which is composed by the transistors Q_3、Q_4 and resistor R_4 starts to work. At the same time, a current mirror is also formed by MOS transistors M_{P14} and M_{P15}. This current mirror makes the PATA current source form a bias circuit and provides a relatively stable bias current for other parts. At this time, the MOS transistor M_{P12} will be turned on, thereby raising the gate potential of M_{P11} and M_{P13}, then the startup is completed, and the startup circuit is closed at the same time.

The magnitude of the bias current can be obtained from the previous Eq. (4):

$$\begin{aligned} I_{Bias} = I_{PATA} &= \frac{V_{BE,Q3} - V_{BE,Q4}}{R_4} \\ &= \frac{V_T}{R_4} \ln M \end{aligned} \tag{6}$$

Wherein, the ratio of the transistors Q_3、Q_4 in parallel is M: 1.

3.2.Bandgap Reference Core Circuit

As shown in Fig.2, the reference voltage can be achieved directly at the output of the five-tube OTA(Operational Transconductance Amplifier). By adjusting the one-stage amplifier, a high-precision output reference voltage that is independent of temperature characteristics can be obtained

From the previous analysis, it's known that X and Y are equipotential. The resistances R_2 and R_3 have the same resistance, so the current flowing through the transistors Q_1、Q_2 can be expressed as

$$I_1 = I_2 = \frac{V_{ref} - V_X}{R_2} \tag{7}$$

The voltage of the output of the operational amplifier is given by Eq. (5):

$$V_{ref} = V_{BE,Q2} + V_T \frac{R_2}{R_1} \ln N \tag{8}$$

Where N is the ratio of the two transistors' number Q_1、Q_2 connected in parallel. Using the coefficient of the positive and negative temperature weighting in Eq. (8), the coefficient relationship

can be adjusted by R_1、R_2, and the reference voltage with temperature-independent characteristics can be obtained.

In the case of room temperature, there are equations $\partial V_{BE} / \partial T \approx -1.5mV / {}^oK$ and $\partial V_T / \partial T \approx +0.087mV / {}^oK$ [2].When $(R_2 / R_1)\ln N \approx 17.2$ comes true, the positive and negative temperature coefficients in Eq. (8) can cancel each other, so that a zero temperature coefficient and high-precision reference voltage are obtained

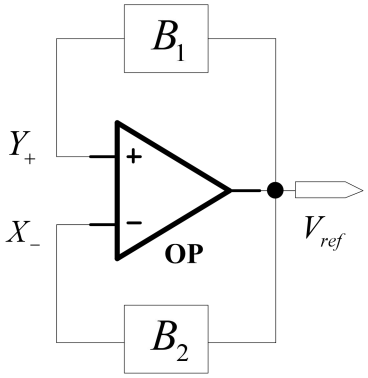

Figure 3: Partial system structure of the bandgap reference.

As shown in Fig.3 the system structure diagram of the bandgap reference, where OP is a five-tube OTA, the gain is A_{VOP} ; a voltage divider network B_1 formed by resistances R_1、R_2 and transistor Q_2, β_1 is a gain; a voltage divider network B_2 formed by R_3 and Q_1, β_2 is a gain. Then the transfer function of this system is:

$$\left[\left(Y_+ - \beta_1 V_{ref}\right) - \left(X_- - \beta_2 V_{ref}\right)\right] A_{VOP} = V_{ref} \tag{9}$$

Then:

$$\frac{V_{ref}}{Y_+ - X_-} = \frac{A_{VOP}}{1 + A_{VOP}\left(\beta_1 - \beta_2\right)} \tag{10}$$

When the gain of the error amplifier is large enough, there is:

$$\frac{V_{ref1}}{Y_+ - X_-} \approx \frac{1}{\beta_1 - \beta_2} \tag{11}$$

And the relevant literature [2] knows:

$$\beta_1 = \frac{r_{Q1}}{R3 + r_{Q1}} \tag{12}$$

$$\beta_2 = \frac{R_1 + r_{Q2}}{R_1 + R_2 + r_{Q2}} \tag{13}$$

In Eq. (12) and Eq. (13), r_{Q1}、r_{Q2} are the small-signal equivalent resistances of the two transistors, and there is the equation $r_{Q1}=r_{Q2}=r_Q$.

The closed-loop gain of the system is:

$$\begin{aligned} |A|_{close-loop} &= \frac{1}{\beta_1 - \beta_2} \\ &= \frac{\left(R_1 + R_2 + r_Q\right)\left(R_3 + r_Q\right)}{R_1 R_3} \end{aligned} \tag{14}$$

3.3.Negative Feedback Circuit

In order to suppress the power supply noise generated by the Buck DC-DC power management system, it is necessary to improve the high power supply rejection characteristic (PSR) of the voltage reference module. The general method is to stabilize the power supply voltage of the voltage reference module, therefore improving the source suppression characteristic. According to this idea, this paper designs the voltage reference core module as an independent part, and then adds it to a closed-loop feedback system. Finally, the negative feedback loop effect of this new closed-loop system can be used to improve the power supply rejection characteristics of the entire circuit.

In the negative feedback part of the overall circuit in Fig.2, after the power supply voltage V_{DD} increases slightly, although the diode connection method M_{P10} will cause the gate grid voltage of M_{P9} to follow the V_{DD} changing, the bias current exists, so this keeps the M_{P9}'s gate-source voltage $V_{GS,MP9}$ stable.

Because the drain-source resistance R_{ds} of the MOS transistor exists, the rise of V_{DD} will cause the current increase. According to Kirchhoff's current theorem, if the M_{P9}'s current flowing out increases, the current flowing into the reference core circuit and the two MOS transistor M_{P8}、M_{N7} will also increase, which will cause a rise in voltage V_{pre}.

From the previous system structure analysis method, it can be found

$$\frac{V_{ref}}{V_{pre}} \approx \frac{PSR_1 \ A_{O2} + PSR_2}{\left|\beta_1 - \beta_2\right| \ A_{O1} \ A_{O2}} = \frac{1}{\left|\beta_1 - \beta_2\right|} \frac{PSR_1 \ A_{O2} + PSR_2}{A_{O1} \ A_{O2}} \tag{15}$$

Putting Eq. (17) into (18), Eq. (18) can become

$$\frac{V_{ref}}{V_{pre}} = \frac{\left(R_1 + R_2 + r_Q\right)\left(R_3 + r_Q\right)}{R_1 R_3} \frac{PSR_1 \ A_{O2} + PSR_2}{A_{O1} \ A_{O2}} \tag{16}$$

From the small-signal model [2], it's known as

$$PSR_1 = \frac{g_{O,MP4}}{2g_{O,MN2}} \tag{17}$$

$$PSR_2 = \frac{g_{O,MP6}}{g_{O,MN3} + g_{O,MP6}} \tag{18}$$

Putting Eq. (17) and (18) into (16) gives

$$\frac{V_{ref}}{V_{pre}} = \frac{\left(R_1 + R_2 + r_Q\right)\left(R_3 + r_Q\right)}{R_1 R_3} \frac{\frac{g_{O,MP4}}{2g_{O,MN2}} A_{O2} + \frac{g_{O,MP6}}{g_{O,MN3} + g_{O,MP6}}}{A_{O1} \ A_{O2}} \tag{19}$$

It can be seen in the above Eq. (19) that both parts of the factor are far less than one, and the product of them is also far less than one, so that the change of the output voltage V_{ref} of the reference circuit is minimal compared with the change in voltage V_{pre}. Therefore, for the MOS transistor M_{P8}, when V_{pre} and V_{ref} change occurring at the same time, the change of the M_{P8}'s gate terminal voltage can be ignored. As a result, the MOS transistor M_{P8} and the bias current I_{Bias1} constitute a group of common-gate amplifiers, and the rise in voltage V_{pre} will cause the output voltage of the common-gate amplifier, so the gate voltage of the MOS transistor M_{N7} will also increase.

If the MOS transistor M_{N7} is used as the input transistor and the remaining circuits are used as a load of this input transistor, a common source amplifier with NMOS output will be formed. Therefore, when the gate voltage of the MOS transistor M_{N7} rises, the voltage V_{pre} at its output terminal will decrease.

Through the above analysis process, the closed-loop system forms a negative feedback loop, which not only enhances the system stability, but also improves the high power supply rejection (PSR) characteristics of the entire reference system.

Assuming that the equivalent resistance from V_{pre} end to the ground is $R_{pre}\left(g_{O,pre}=1/R_{pre}\right)$, through the Thevenin's Equivalent Voltage Theorem, it can be got

$$V_{DD}\frac{g_{O,MP9}}{g_{O,MP9}+g_{O,pre}}-V_{pre}\left(1-\frac{V_{ref}}{V_{pre}}\right)\left(\frac{g_{M,MP8}}{g_{O,MP8}}\right)\frac{g_{O,MN7}}{g_{O,MP7}+g_{O,pre}}=V_{pre} \tag{20}$$

From Eq. (23), it can be concluded:

$$\frac{V_{pre}}{V_{DD}}\approx\frac{g_{M,MP9}\ g_{O,MP8}}{g_{M,MP8}\ g_{O,MN7}} \tag{21}$$

Combining Eq. (19) and Eq. (21), the gain between the power supply voltage of the negative feedback part and the output reference voltage is shown

$$\frac{V_{ref}}{V_{DD}}=\frac{\left(R_1+R_2+r_Q\right)\left(R_3+r_Q\right)}{R_1R_3}\frac{\frac{g_{O,MP4}}{2g_{O,MN2}}A_{O2}+\frac{g_{O,MP6}}{g_{O,MN3}+g_{O,MP6}}}{A_{O1}A_{O2}}\frac{g_{M,MP9}\ g_{O,MP8}}{g_{M,MP8}\ g_{O,MN7}} \tag{22}$$

By comparing Eq. (19) and Eq. (22), it can be seen that based on the original bandgap core circuit, adding a negative feedback loop makes the obtained gain reduce, so that the new circuit's gain is about square of the MOS's intrinsic gain. By adding a negative feedback loop module to the original reference circuit, not only the gain of the entire system is improved, but also the negative feedback characteristic of the system is strengthened. This way makes the system more stable and capable of outputting a more stable reference voltage, which better achieves the Converter's step-down operation.

4. Result of Simulation

The circuit designed in this paper uses TSMC 65nm CMOS technology, and uses Virtuoso Spectre in Cadence's IC simulation tool to simulate in the temperature range of -40℃ ~ 90℃.

In the overall circuit of Fig.2, when the power supply voltage is turned on, the whole circuit is started. When the power supply voltage changes from 0 to 5.5V, it can be seen that the reference circuit can normally work at 3V power supply voltage, and the output is stable at around 1.23V.

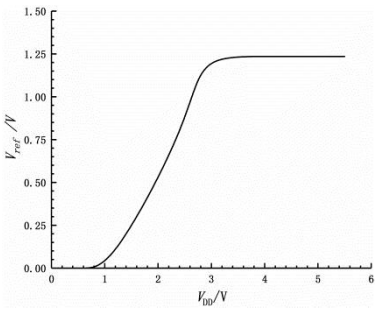

Figure 4: Change curve of output reference voltage with power supply voltage.

Fig.5 is the temperature characteristic curve of the bandgap reference voltage under the tt model. As can be seen from the figure, when the ambient temperature changes from -40℃ to 90℃, the temperature coefficient of this circuit can be calculated.

$$T = \frac{V_{\max} - V_{\min}}{V_{\min}\left(T_{\max} - T_{\min}\right)} = 5.3\times10^{-6} \quad \text{.....} \tag{23}$$

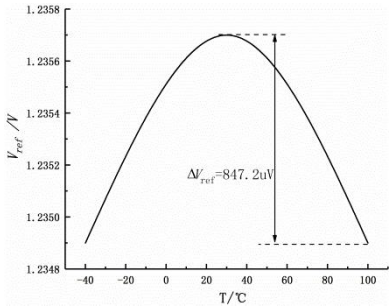

Figure 5: Temperature characteristics of bandgap reference voltage.

When the input voltage is 5V, the power supply rejection ratio (PSRR) simulation result of the entire reference system is shown in Fig.6. It can be seen from the simulation results that at low frequencies, the power supply rejection ratio is basically stable around -65.8dB.

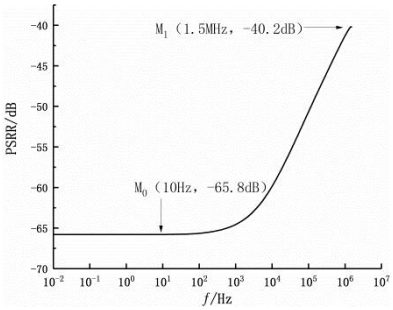

Figure 6: Power supply rejection characteristics of the bandgap reference circuit.

By comparing the parameters of the circuit designed in this paper with other works of literature, the comparison shown in Table 1 can be obtained. As can be seen from the this, the circuit proposed in this article has a lower temperature coefficient in a wide range of temperature changes (-40 ℃ to 90 ℃), and an excellent power supply suppression characteristics are shown in a wide range of frequency changes (0 to 1.5MHz). Working in a typical environment of 3~5.5V, it is very suitable for Buck DC-DC converter.

Table 1: Comparison of the simulation results of the circuit in this paper with other literatures.

	This design	K. Peng et al[6]	K. Ueno et al [7]	Y. Chen et al[8]
Process	65nm CMOS	65nm CMOS	0.35um CMOS	0.5um CMOS
Temp Rang/℃	-40~90			-40~85
Supply voltage/V	3-5.5	1.2	1.4-3	3.3
Temperature Coefficient/ppm/℃	5.3	9.6	15	11.6
PSRR/dB	-65.8	-73	-45	-69

5. Conclusions

Based on the design requirements of the Buck DC-DC converter, this paper designs a high-performance CMOS bandgap reference voltage source with negative feedback network loop. This bandgap reference source operates at a temperature of-40℃~90℃ and shows relatively stable output voltage characteristics. The temperature coefficient and PSRR (power supply rejection ratio) is better than similar circuits. The overall circuit design is based on a traditional bandgap reference circuit, adding one-stage op amps adjusting parameters, and adding a negative feedback loop to effectively ensure the stability of the output reference voltage.

Acknowledgments

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